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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,863	01/10/2002	Chung-Liang Chang	TS01-603	8427

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EXAMINER

CHEN, KIN CHAN

ART UNIT

PAPER NUMBER

1765

DATE MAILED: 05/01/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/043,863

Applicant(s)

CHANG ET AL.

Examiner

Kin-Chan Chen

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-37 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 15 and 35 are objected to because of the following informalities:

In claims 15 and 35, the examiner suggests deleting "(CMP)" because it might have several meanings.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. Claims 2 and 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 2 and 3, semiconductor material comprising photoresist (I-line or DUV) is vague and indefinite because photoresist is not semiconductor material.

Claim Rejections - 35 USC § 103

3. Claims 1-12, 17-32, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (US 6,251,774; hereinafter "Harada").

In a method of forming a dual damascene structure, Harada teaches providing a substrate with at least one point of electrical contact, a layer of IMD, at least one opening being aligned with the point of electrical contact; depositing a layer of first photoresist material over the surface of IMD, filling at least one opening created through the layer of IMD; removing the layer of first photoresist material from the surface of the layer of IMD, thereby removing the first photoresist from at least one opening created through the layer of IMD, creating at least one partial opening through the IMD; baking the substrate for a period of time by applying an elevated temperature in a gaseous environment and under pressure to the substrate (col. 6 and col. 7, lines 15-17). Harada teaches that a BARC may be deposited before depositing a layer of second photoresist over the surface of the layer of IMD. It is known in the art of semiconductor device fabrication that BARC is optionally applied under the photoresist to ensure that no light is reflected back from the chip surface into photoresist and to avoid exposure-disturbing. Therefore it can be omitted as instantly claimed invention. Without BARC, Harada teaches the method comprising depositing a layer of the second photoresist over the surface of the layer of IMD, thereby filling the at least one partial opening created through the layer of IMD and patterning and etching the layer of the second photoresist; creating an opening through the layer of the second photoresist that aligns with the at least one partial opening created through the layer of IMD, removing the layer of second photoresist from the at least one partial opening created through the layer of IMD.

As to dependent claims 2, 3, 20, and 23, Harada is not particular about the photoresist used in the process. Hence, it would have been obvious to one with ordinary

skill in the art to use said photoresists because they are commonly used in the art of semiconductor device fabrication.

The above cited claims differ from the prior art by specifying well-known features (such as using hot plate or furnace for baking in claims 4, 5, 24, 25; applying wet etch for creating an opening in IMD in claims 17 and 37) to the art of semiconductor device fabrication. A person having ordinary skill in the art) would have found it obvious to modify Harada by adding any of same well-known features to same in order to provide their art recognized advantages and produce an expected result.

The above cited claims differ from the prior art by specifying various processing parameters (such as baking temperatures, pressure, and period of time in claims 6-8, 12, 26-28, and 32). However, they are commonly determined by routine experiment. The process of conducting routine optimizations so as to produce an expected result is obvious to one of ordinary skill in the art. Hence, it is the examiner's position that a person having ordinary skill in the art at the time of the claimed invention would have found it obvious to modify Harada by performing routine experiments to obtain optimal result.

4. Claims 13-16 and 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (US 6,251,774; hereinafter "Harada") as applied to claims 1-12, 17-32, and 37 above, and further in view of Chooi et al. (US 6,284,657; hereinafter "Chooi") or Chung et al. (US 6,017,817; hereinafter "Chung").

The discussion of modified Chooi from above is repeated here.

Harada teaches forming dual damascene structure, but does not detail the conventional damascene structure forming steps. Chooi or Chung is relied on only to show some conventional process steps such as depositing copper, filling the opening, removing the copper from the surface of the substrate using CMP. Because it is a conventional method to form dual damascene and because it is disclosed by Chooi or Chung, it would have been obvious to one with ordinary skill in the art to use same in the process of Harada in order to provide their art recognized advantages and produce an expected result.

Conclusion

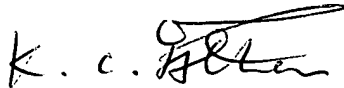
5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chang (US 5,643,407; col. 4, lines 45-48) teaches that baking semiconductor substrate may be performed in a nitrogen ambient at temperature about 250 °C to 350°C for between 20-40 minutes.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kin-Chan Chen whose telephone number is (703) 305-0222. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on (703) 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-2934.

A handwritten signature in black ink, appearing to read "K. C. Allen". The signature is written in a cursive style with a long horizontal stroke extending from the end.

K-C C
April 24, 2003

Patent Examiner
Group Art Unit 1765